Alumni Guest Lecture Report

Guest Lecture Title**: ENTREPRENEURSHIP OPPORTUNITIES IN 'VLSI'**

Guest Speaker: Dr R ASHOK KUMAR REDDY
Correspondent, Tadipatri Engineering college
Batch: B –TECH (2004 -2008).

Date: 0**3.12.2022.**

Time: 10**:00 PM – 12:00 PM.**

Total Participants: 120 (Second Year ECE Students).

Participated Faculties**: Dr. Rajasekaran (HoD - ECE)**

Dr. P. Ramesh Reddy (Alumni Relation Officer)

Mr. E. Ramesh (Department Alumni Coordinator),

About Speaker:

Dr R ASHOK KUMAR REDDY is a distinguished Bachelor Degree Alumni of MITS, After his Bachelor degree, he completed his masters and P.hd from JNTU Anantapur, He is know action as correspondent of tadipatri engineering college and also cofounder Broad semiconductors Pvt.Ltd

Objective
The aim of this guest lecture was to know Entrepreneurship opportunities in VLSI and recent technologies Development VLSI

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The program started at 10:00 am. Dr. P. Ramesh Reddy – HOD& Alumni Relation Officer, Department of Mathematics, Dr. S. Rajasekaran (HoD - ECE), Dr Dr R ASHOK KUMAR REDDY were invited on to the dais.

Dr. S. Rajasekaran motivated the students to make utilize of the lecture in his introductory speech and appreciated the Management for providing all benefits for the students to motivated by their senior Alumni. He conveyed best wishes to the resource person to handle the guest lecture.

Dr. P. Ramesh Reddy conveyed message that the students have to utilize the opportunities provided by the management and the faculty in bringing distinguished alumni for Guest lecture which will help grow them even as Entrepreneur.

The distinguished Alumni Dr Ashok Kumar Reddy Explained his studious and how he faced struggling to speak English in his Bachelor and he explained how to overcome inferiority complex, and he explained his motivation to became as Entrepreneur as tadipati local he wants enrich his town as educational hub he established engineering college, All the students are in the right time of the globalization process. Industry 4.0 is gaining more and more attention towards all the top companies in the technology. As a ECE students VlSI has a market of 3 trillion-dollar business in next coming 5 years around the globe he said it is time to young Entrepreneurs it is good opportunity, he told during the past decade the VLSI design and prototyping area has developed lot of traction Lot of new innovative ideas are floated in the market. In the present scenario, there are most of the feasible ideas on which engineers are working on in various streams Most of the engineers during last year wanted to implement the practical oriented ideas. As an entrepreneur we have initiate support their thoughts by delivering the training in such areas because the main worry is the real awareness of VLSI domain areas and the availability of experts and professionals.

He explained different streams in VLSI

- **RTL Design and Verification**

RTL is expressed in a Hardware Description Language (HDL), such as VHDL or Verilog. This description can be used in simulation and verification

- **Physical design**

In many cases, physical design can be completely or partially automated and layout can be generated directly from netlist by Layout Synthesis tools. Layout synthesis tools, while fast, do have an area and performance penalty, which limit their use to some designs

- **Fabrication**

A large wafer is 20 cm (8 inch) in diameter and can be used to produce hundreds of chips, depending of the size of the chip. Before the chip is mass produced, a prototype is made and tested

- **Design for Testability(DFT)**

  The chip manufacturing process is prone to defects and the defects are commonly referred as faults. A fault is testable if there exists a well-specified procedure to expose it in the actual silicon.

  To make the task of detecting as many faults as possible in a design, we need to add additional logic; Design for testability (DFT) refers to those design techniques that make the task of testing feasible. In this article we will be discussing about the most common DFT technique for logic test, called Scan and ATPG

He told that in India fabrication not possible but know Indian government efforts about make in India next decade India is going to reach china in fab industry as off know we have good opportunity as entrepreneurs

The session concluded with vote of thanks by coordinators